CS98-106,7,8

GAP FILLING PROCESS IN INTEGRATED CIRCUITS USING LOW DIELECTRIC CONSTANT MATERIALS

B1
Ins 91

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to a method of fabrication used for semiconductor integrated circuit devices, and more specifically it relates to structures for reducing capacitance between closely spaced interconnection lines of integrated circuits. In particular, it pertains to structures and methods for improving adhesion and preventing micro cracks in low dielectric constant materials when used in conjunction with conventional dielectric materials as intermetal dielectrics (IMD).

(2) DESCRIPTION OF PRIOR ART

Integrated circuits and the progress made in Silicon Technology has continued to shrink the size of devices. This has led to closer and closer spacing of interconnection lines. As spacing becomes closer, the capacitance between adjacent lines has increased, as device geometries shrink and circuit densities increase. The capacitance between

lines is directly related to both the distance between the lines and dielectric constant of the material in between the lines. Hence, a low dielectric material between the closely spaced interconnect lines is beneficial in reducing the capacitance.

In 0.25 micron, or below (e.g., 0.18, 0.13 um), technology the performance is limited by the interconnect line delay, with line-to-line capacitance being greatly affected by RC delay of the lines, as line width and line space becomes less than about 0.3 microns. Therefore, the introduction of low dielectric materials between the closely spaced interconnect, transmission lines can greatly enhance the integrated circuit performance in terms of speed, by lowering the RC time constants.

U.S. Patent 5,818,111 entitled "Low Capacitance Interconnect Structures in Integrated Circuits Using a Stack of Low Dielectric Materials" granted Oct.6, 1998 to Jeng and Taylor describes a method and structure for integrating hydrogen silsesqui-oxane (HSQ) and other low dielectric materials, which have undesirable properties, into integrated circuit structures and processes. A stabilizing

layer is inserted between layers of low dielectric constant films. A layer of low dielectric constant HSQ is spun over and in between metal interconnect lines with a thin layer of silicon dioxide used as a stabilizing layer on top. Alternating layers of HSQ and thin silicon dioxide are fabricated together with multilevel metal structures. Finally, a thick silicon dioxide layer for planarization is placed on top of the multi-level metal layer structures.

US Patent 5,759,906 entitled "Planarization Method for Intermetal Dielectrics Between Multilevel Interconnections on Integrated Circuits" granted Jun. 2, 1998 to Lou describes a method for making a planar intermetal dielectric layer (IMD) for multilevel electrical interconnections on ULSI circuits. The method involves forming metal lines on which is deposited a conformal PECVD oxide. A multilayer of spin-on glass (SOG), composed of at least four layers, is deposited and baked at elevated temperatures and long times after each layer to minimize the poisoned via problem. After depositing a silicon dioxide layer on the SOG, the layer is partially chemical/mechanically polished to provide the desired, more global planar, IMD. The method can be repeated for multilevel metal lines.

US Patent 5,385,866 entitled "Polish Planarizing Using Oxidized Boron Nitride as a Polish Stop" granted Jan. 31, 1995 to Bartush shows a method of polishing of a non-planar surface layer on a semiconductor substrate using an oxidized boron nitride polishing stop layer. The oxidized boron nitride polish stop layer is selectively polished relative to the non-planar surface layer. The oxidized boron nitride acts as a polishing stop layer for the process over an FET gate structure.

US Patent 5,821,621 entitled "Low Capacitance Interconnect Structure for Integrated Circuits" granted Oct. 13, 1998 to Jeng shows a method for integrating polymer and other low dielectric constant materials, which may have undesirable physical properties, into integrated circuits structures and processes, especially those requiring multiple levels of interconnect lines. It combines the use of silicon dioxide with low dielectric constant materials. The low dielectric constant materials are spun-on and defined by photolithography to be only in the critical areas between interconnect lines. After planarization, the process steps can be repeated for multiple interconnect layers.

SUMMARY OF THE INVENTION

It is the general object of the present invention to provide an improved method of fabricating semiconductor integrated circuit devices, specifically by describing an improved process of fabricating multilevel metal structures using low dielectric constant materials. Furthermore, the present invention relates to an improved method for fabricating stable and planar intermetal dielectric materials, using low dielectric constant materials.

The method by the first embodiment of this invention, uses a stabilizing adhesion layer between the bottom, low dielectric constant layer and the top dielectric layer. The advantages of the stabilizing adhesion layer are: (i) improved adhesion and stability of the low dielectric layer and the top dielectric oxide (ii) over all layer thickness of the dielectric layers can be reduced, hence lowing the parasitic capacitance of these layers.

In the second embodiment of the present invention, the method uses a multi-layered "hard mask" on metal interconnect lines with an underlying silicon oxynitride DARC, dielectric anti-reflective coating. The term hard mask

refers to these layers that exhibit resistance to being chemical-mechanical polished (CMP) back in the planarization process. A double coating scheme of low dielectric constant insulators are used in this application of the invention. Several advantages are achieved by this method: (i) improved global planarization with low dielectric constant material used in conjunction with hard mask (ii) adhesion and stabilizing material used between low dielectric material and oxide dielectric (iii) double coat of low dielectric material for whole interlevel metal dielectric (IMD) stack.

Still another object of this invention, is the third embodiment of the present invention, a multi-layered hard mask stack over the interconnect metal lines with silicon oxynitride DARC, dielectric anti-reflective coating, is used, and in addition, an adhesion and stabilization layer is used between the low dielectric material and the top dielectric layer. In this application of the invention, several advantages are achieved: (i) improved global planarization (ii) reduction of outgassing and via poisoning (iii) easy integration of low dielectric constant material.

The present invention starts with conventional processing of the semiconductor substrate and continues with conventional processing up to the fabrication of the first level of metal interconnect lines. A detailed description of the aforementioned conventional processing is found in the section titled, "DESCRIPTION OF THE PREFERRED EMBODIMENTS".

Integrated circuits and the progress made in Silicon Technology has continued to shrink the size of devices. This has led to closer and closer spacing of interconnection lines. As spacing becomes closer, the capacitance between adjacent lines has increased, as device geometries shrink and circuit densities increase. The capacitance between lines is directly related to both the distance between the lines and dielectric constant of the material in between the lines. Hence, a low dielectric material between the closely spaced interconnect lines is beneficial in reducing the capacitance.

In quarter micron technology and below, the performance is limited by the interconnect line delay, with line-to-line capacitance being greatly affected by RC delay of the lines, as line width and line space becomes less than about 0.3 microns.

Therefore, the introduction of low dielectric materials between the closely spaced interconnect, transmission lines can greatly enhance the integrated circuit performance in terms of speed, by lowering the RC time constants.

This invention relates to a method of fabrication used for semiconductor integrated circuit devices, and more specifically it relates to structures for reducing capacitance between closely spaced interconnection lines of integrated circuits. In particular, it pertains to structures and methods for improving adhesion and preventing micro cracks in low dielectric constant materials when used in conjunction with conventional dielectric materials as intermetal dielectrics (IMD).

In the first embodiment of the present invention, conventional processing is used to fabricate the interconnect metal lines, which are defined on an interlevel dielectric layer (ILD) on a semiconductor substrate. A low dielectric constant material is then deposited on and in between the metal interconnect lines. Key to the process is the deposition of a thin non-oxide dielectric adhesion and stabilization layer, such as, silicon nitride, which is deposited on top of the low dielectric constant layer. Other

adhesion and stabilization layers can be used, e.g., chemical vapor deposition (CVD) of SiC and related compounds of BC, BCN, BN or spun on materials . A cap silicon oxide is deposited onto the adhesion and stabilization layer and this cap oxide helps to planarize the surface. Further planarization of the surface is achieved by then chemical-mechanical polishing (CMP) of the top cap oxide. Finally in the process, via openings to contact the metal below are fabricated by defining the via area by photolithography and then etching the openings through: cap oxide, thin adhesion layer and then through the low dielectric material. Conductive metal is deposited into the via opening to connect the metal lines below. The excess conductive metal is then removed and the surface planarized by chemical-mechanical polish (CMP).

In another embodiment of the present invention, a multi-layered "hard mask" with silicon oxynitride DARC, dielectric anti-reflective coating, is used on top of metal. The term hard mask refers to the layers resistance to being chemical-mechanical polished (CMP) back. A layer of metal is deposited on the interlevel dielectric layer (ILD) and then a multi-layered hard mask layer, e.g., silicon nitride and silicon oxide layers, are deposited on top of the metal

layer. This multi-layered hard mask layer, with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal, can just be silicon nitride alone, or just silicon oxide, or can be the combination of both silicon nitride and silicon oxide. Next in the process is the masking and etching of the interconnect metal lines. Now with the hard mask in place over the defined metal lines, with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal, a low dielectric constant layer is deposited over the surface and cured by a curing process. The low dielectric constant material is chemical-mechanical polished (CMP) back with the multi-layered hard mask in place over the metal with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal. The surface is planarized by the CMP and the CMP process stops on the hard mask, removing some of the hard mask in the process, e.g., silicon oxide. Some of the hard mask remains as the silicon nitride layer. At this stage in the process, this invention branches off into two separate embodiments. One embodiment involves a another coating (the second) of low dielectric constant material and followed by the deposition of another single or multiple layers of hard mask material on top of low dielectric constant material. The other embodiment, which branches off involves the use of an adhesion promoter

and stabilization layer in between thicker cap oxide and low dielectric layer. Combinations of these two branch processes can also be applied. A more detailed description of each branch is given in the next few paragraphs.

In the second embodiment of the invention, the process follows the same scheme described above using the hard mask process. Next, a second layer of low dielectric constant material, or double coating, is applied over a hard mask, which consisting of a non-oxide dielectric layer, such as, silicon nitride. Another hard mask layer, for low dielectric constant via open is deposited over the second low dielectric layer. This second hard mask layer can be composed of just silicon nitride, or just silicon oxide or both materials. This process is followed by via definition and etching for via openings. Conductive metal is deposited and excess metal is chemical-mechanical polished (CMP) back to form electrically conductive vias to the interconnect metal lines below.

In the third embodiment of the invention, the process follows the same scheme described above using the hard mask process. A thin layer of adhesion promoter, silicon nitride, is deposited both over the hard mask and the low dielectric

constant layer. Next a cap oxide layer is deposited. This process is followed by via definition and etching for via opening. Conductive metal is deposited and excess metal is chemical-mechanical polished (CMP) back to form electrically conductive vias to the interconnect metal lines below.

In summary, several embodiments of this invention were described: (i) the use of a non-oxide dielectric adhesion promoter for cap oxide (ii) the use of a double coating of low dielectric constant material and multi-layered hard mask material (iii) the use of a hard mask material, in combination with, the use of an adhesion promoter for cap oxide. Other combinations of the above embodiments are possible and should be understood as part of this invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the description of the preferred embodiments with reference to the attached drawings that include:

Figure 1a which in cross-sectional representation

illustrate the prior art method of forming low dielectric constant gap fill.

Figure 2 a-d illustrates one embodiment of the present invention using a non-oxide adhesion layer between dielectric layers.

Figure 3 a-d illustrates another set of embodiments of the present invention using multi-layered hard mask process.

Figure 4 a,b illustrates use of a hard mask and double coating of low dielectric material.

Figure 5 a,b shows the use of a hard mask in conjunction with an adhesion layer for dielectrics.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention relates to a method for fabricating planar intermetal dielectric materials. The method by the first embodiment uses a stabilizing adhesion layer between the bottom low dielectric constant layer and top dielectric layer. In the second embodiment of the

present invention, the method uses a multi-layered "hard mask" on metal interconnect lines with a silicon oxynitride DARC, dielectric anti-reflective coating on top of metal. The term multi-layered hard mask refers to these layers that exhibit resistance to being chemical-mechanical polished (CMP) back in the planarization process. In the third embodiment of the present invention, a hard mask stack over the interconnect metal lines with silicon oxynitride DARC, dielectric anti-reflective coating, on top of metal, is used, and in addition, an adhesion and stabilization layer is used between the low dielectric material and the top dielectric layer.

As background to the present invention, a conventional method of fabricating intermetal dielectric (IMD) is illustrated as Prior Art in a cross-sectional sketch in Figures 1. As shown in Figure 1, a semiconductor substrate 1 is the base starting material, such as single-crystal silicon on which are formed semiconductor devices. The devices are not shown in the Figs. to simplify the drawings and the discussion. For example, the method can be applied to integrated circuits having devices such as field effect transistors (FET's), bipolar transistors and the like made in and on the substrate surface. A first insulating layer 2

is deposited over the substrate 1 having semiconductor devices. Preferably the first insulating layer is composed of a silicon oxide (SiO_2) and is deposited by low pressure chemical vapor deposition (LPCVD), or by sub-atmospheric chemical vapor deposition (SACVD), using a reactant gas such as tetraethosiloxane (TEOS) and oxygen (O_2) or ozone (O_3). Preferably layer 2 is deposited to a thickness of between about 5000 and 10000 Angstroms. Layer 2 serves as the pre-metal interlevel dielectric (PMD) that provides electrical insulation of the devices from the level of metal interconnections that are made next.

Contact openings (not shown in Figs.) are etched in the first insulating layer 2 to form oontacts to the devices, such as source/drain contact areas and gate electrodes of FET's, or to emitter, base and collector areas of bipolar devices. The contacts can be etched, for example, by high-density plasma (HDP) etching in an etchant gas such as trifluoromethane (CHF_3), which selectively etches the oxide to the silicon substrate 1. A barrier layer, which is not explicitly depicted in the Figs., is deposited over the first insulating layer 2 and in the contact openings. The barrier layer, typically composed of titanium (Ti)/titanium nitride (TiN) or titanium tungsten (TiW) is used to prevent

aluminum penetration into the shallow junctions of the devices and to improve adhesion. A first conductive layer is now deposited and patterned to form defined interconnect metal lines 4, (with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal), on the surface of a silicon oxide layer 2, the interlevel dielectric layer (ILD). A low dielectric constant, low k, material 6 is deposited over and in between the interconnect metal lines 4. Over the low dielectric material is a deposited "cap silicon oxide layer" 8 that helps to planarize the surface and can be chemical-mechanical polished (CMP) back to further planarize the surface. Multilevel interconnect metal line structures, with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal, can be fabricated by this method. The low dielectric constant material in between and around the interconnect metal lines reduces the parasitic capacitance of the metal lines and hence increases signal speed and performance by lowering the RC time constant of the lines.

Several problems arise by this conventional method, shown in Fig. 1. One main concern is the adhesion of the cap oxide 8 to the underlying layer of low dielectric constant material 6. Other concerns are the introduction of reaction

gases that include oxygen and nitrous oxide gases prior to the cap oxide deposition. These gases are necessary for reaction chamber stabilization and react with the surface of the low dielectric constant layer, making adhesion of the subsequent cap oxide worse. The present invention solves these problems, as described in the following section, starting with Figure 2.

As shown in Fig. 2a, the interconnect metal lines 4 are defined on a semiconductor substrate 1 with an interlevel dielectric layer (ILD) 2, all with conventional processing. In Fig. 2b, one embodiment of the present invention is illustrated, showing a low dielectric constant material deposited on and in between the metal lines 4, but now a thin non-oxide adhesion layer, such as, silicon nitride 7 is deposited on top of the low dielectric constant layer 6. Other adhesion layers can be used, e.g., chemical vapor deposition (CVD) of SiC and related compounds of BC, BCN, BN or spun on materials .

The low dielectric constant material is spun on dielectric (SOD), especially useful are organic compounds, which are coated by the spin on method to a thickness from about 4,000 to 12,000 Angstroms. Curing conditions are: 1

hr. at 400°C, in a nitrogen ambient, with gas flow of between 1 to 30 LM. The low dielectric constant material has a dielectric constant of less than 2.8.

The deposition conditions of the non-oxide, dielectric layer, such as, the silicon nitride layer are, plasma enhanced chemical vapor deposition (PECVD): film thickness from about 200 to 500 Angstroms, temperatures from about 300 to 400°C, deposition rates from about 900 to 8,000 Angstroms/min, ammonia gas flow from about 80 to 200 sccm and silane gas flow from about 200 to 350 sccm, with pressures from about 1 to 10 Torr, RF power from about 400 to 800 Watts.

In Fig. 2c is sketched the cap silicon oxide 8 is deposited onto the adhesion layer 7 and this cap oxide helps to planarize the surface. Further planarization of the surface is achieved by then chemical-mechanical polishing (CMP) of the top cap oxide, as shown is Fig. 2c. Finally in the process, Fig. 2d, via openings are fabricated by defining the via area 12 by photolithography and then etching the openings through: cap oxide 8, thin adhesion layer 7 and low dielectric material 6. Conductive metal 14 is deposited into the via opening to connect the metal lines

below. The excess conductive metal is then removed and the surface planarized by chemical-mechanical polish (CMP), as shown in Fig. 2d. The cap oxide is silicon oxide deposited by plasma enhanced chemical vapor deposition (PECVD), in the thickness range from about 4,000 to 16,000 Angstroms, and having a dielectric constant of about 4.0.

Another embodiment of the present invention is illustrated in Fig. 3. It can be termed, a multi-layered "hard mask" on metal with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal stack. The term hard mask refers to the layers resistance to being chemical-mechanical polished (CMP) back. As shown in Fig. 3a, a layer of metal is deposited on an interlevel dielectric layer 2 and then a hard mask layer of silicon nitride 7 and silicon oxide layer 9 are deposited. This multi-layered hard mask (with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal stack) can just be silicon nitride alone, or just silicon oxide, or can be the combination of both silicon nitride 7 and silicon oxide 9, as shown in Fig. 3a.

The silicon nitride deposition is the same, as described earlier, for plasma enhanced chemical vapor

deposition (PECVD), with nitride thickness from about 200 to 500 Angstroms. The deposition conditions for the silicon oxide above are the following, plasma enhanced chemical vapor deposition (PECVD): film thickness from about 1,000 to 2,000 Angstroms, silane gas flow from about 70 to 200 sccm, nitrous oxide gas flow from about 1,500 to 3,000 sccm, pressure from about 1 to 10 Torr, temperature from about 300 to 400°C, and RF power from about 50 to 100 Watts.

Next in the process is the masking and etching of the interconnect metal lines, as illustrated in Fig. 3b. Now with the hard mask 16 in place on the metal lines, a low dielectric constant layer 18 is deposited over the surface and cured by a curing process. This low dielectric material is a carbon based organic polymer, in a thickness range from about 4,000 to 10,000 Angstroms, spun on at spin speeds from about 2,000 to 4,000 rpm for a time of 1 minute. The curing process is at 400°C, for 1 hr., in ambient of nitrogen gas with flows from about 1 to 30 sccm and limiting oxygen concentrate to less than 10 ppm.

In Fig. 3d, the low dielectric constant material 18 is chemical-mechanical polished (CMP) back with the hard mask 16 in place over the metal. The surface is planarized by the

CMP and the process stops on the hard mask, removing some of the hard mask, e.g., silicon oxide, in the process. As shown in Fig. 3d, some of the hard mask remains as the silicon nitride layer 20. At this stage in the process, this invention branches off into two separate embodiments. One embodiment involves a double coating of low dielectric material and the deposition of single or multiple layers of hard mask material, as sketched in Fig. 4a and Fig. 4b. The other embodiment branches off to using an adhesion promoter and stabilization layer for cap oxide over both a hard mask stack and over low dielectric oxide, illustrated in Fig. 5a and Fig. 5b. Combinations of these two branch processing schemes can also be applied. A more detailed description of each branch is given in the next few paragraphs.

As stated above, the process follows the scheme described and shown in Figures 3a-d. Then as illustrated in Fig. 4a, a second layer of low dielectric constant material 22, or double coating, is applied over a hard mask 20 consisting of silicon nitride. Next another hard mask layer is deposited, Fig. 4a over the second low dielectric layer. This second hard mask layer 24 can be composed of just silicon nitride, or just silicon oxide or both materials. This process is followed by via definition and etching for

via opening 26, as shown in Fig. 4b. Conductive metal is deposited and excess metal is chemical-mechanical polished (CMP) back to form electrically conductive vias (26) to the interconnect metal lines (4) below.

The process for the second low dielectric constant material above, is the same as described before, organic based polymer, spun on dielectric (SOD) with a thickness from about 4,000 to 12,000 Angstroms and with the curing conditions the same as described before. The second hard mask process conditions are the same as in the first hard mask process, described before.

The process conditions for via opening is the following: reactive ion etch (RIE) for low dielectric constant via opening, RF power from about 800 to 1,500 Watts, pressure from about 300 to 800 milli-Torr, reactive gases and flow rates N_2 from about 100 to 300 sccm, H_2 from about 100 to 300 sccm, C_4F_8 from about 1 to 10 sccm.

The process conditions for the opening of the first hard mask layer are as follows: reactive ion etch (RIE), RF power from about 300 to 1,000 Watts, pressure from about 30 to 100 milli-Torr, gases and flows CH_2F_2 from about 10 to 50

sccm, O_2 from about 10 to 30 sccm, Ar from about 50 to 200 sccm.

As stated above, the next embodiment of the process follows the same scheme as described and shown in Figures 3a-d. Then as illustrated in Fig. 5a, a thin layer of non-oxide adhesion promoter 7, e.g., silicon nitride, is deposited both over the hard mask 20 and the low dielectric constant layer 18. Next a cap oxide layer (28) is deposited, shown in Fig. 5a. This process is followed by via definition and etching for via opening 30, as shown in Fig. 5b. Conductive metal is deposited and excess metal is chemical-mechanical polished (CMP) back to form electrically conductive vias (32) to the interconnect metal lines (4) below.

In summary, several embodiments of this invention were described: (i) the use of a non-oxide adhesion promoter for cap oxide, as illustrated in Figure 2 a-d, (ii) the use of a double coating of low dielectric material and double hard mask material, as illustrated in Figure 3 a-d and Figure 4 a,b, (iii) the use of a hard mask material (with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal stack), in combination with, the use of an adhesion

promoter for cap oxide, as sketched in Figure 3 a-d and Figure 5 a,b. Other combinations of the above embodiments are possible and should be understood as part of this invention, as stated in the next paragraph below.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: